REMARKS

In the Office Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,872,044 ("*Hemmenway*") in view of U.S. Patent 6,060,749 ("*Wu*") and rejected claims 1 and 2 under § 103 over U.S. Patent 6,017,801 ("*Youn*") in view of *Wu*.

Amendment

Applicant has amended claim 1 to more particularly recite Applicant's invention.

Rejection over *Hemmenway* in view of *Wu*

To establish a *prima facie* case of obviousness under §103(a), each of three requirements must be met. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art," to combine references or modify a reference. (MPEP § 2143 (8th ed. Rev. Feb. 2003).) Second, a reasonable expectation of success must exist that the proposed modification will work for the intended purpose. (*Id.*) Moreover, both of these requirements must "be found in the prior art, not in applicant's disclosure." (*Id.*) Third, the reference or references, taken alone or in combination, must disclose or suggest every element recited in the claims. (*Id.*)

Hemmenway discloses a method for trench isolation. The method includes sequentially performing local oxidation of a wafer to form a gate oxide 4 (*Hemmenway*, col. 4, ll. 39-53), forming a polysilicon gate 31 and source and drain regions 42 and 43, respectively (*id.*, col. 4, l. 50-67), forming an oxide layer 51 and a photoresist layer 61 (*id.*, col. 5, ll. 7-14), forming an opening 62 and a trench 72 (*id.*, col. 5, ll. 14-26), and filling the trench 72 with polysilicon 82 (*id.*, col. 5, ll. 45-47). The trench may be doped

by siliciding the sidewalls of the trench to render them conductive 73. (*Id.*, col. 5, ll. 21–31; Figure 7.) The doped sidewalls 73 may provide suitable contacts to buried layer 2 in bulk material 14. (*Id.*, co. 5, ll. 31–34.) That is, *Hemmenway* discloses doping sidewalls of a trench to contact a buried layer and bulk material.

Wu discloses forming a MOSFET on a SOI substrate. The MOSFET includes a SOI structure 4 on substrate 2. (*Wu*, col. 3 ll. 25–26; Figure 4.) Source/drain regions 26 are on SOI structure 4 and first silicide layer 34 is on source drain regions 26. (*Id.*, col. 3, ll. 40–43; Figure 14.) Also on SOI structure 4 are LDD regions 28, in contact with second isolation structure 32, which are next to first isolation structure 22 around gate 24, under second silicide layer 36. (*Id.*, col. 3, ll. 28–40; Figure 14.) That is, *Wu* discloses a first silicide layer on a source drain region, in turn, on SOI structure.

Hemmenway's doping sidewalls of a trench to contact a buried layer and bulk material and a *Wu's* first silicide layer on a source drain region, in turn, on SOI structure, however, are different from "a first silicide layer disposed at an *interface of the impurity junction region and the device isolation film*," as recited in claim 1 (emphasis added), which further recites, "a device isolation film disposed in the second silicon layer, wherein the device isolation film defines an active region of the SOI wafer." That is, both *Hemmenway* and *Wu* fail to teach or suggest, at least, "a first silicide layer disposed at an interface of the impurity junction region and the device isolation film," as recited in claim 1.

Moreover, Applicant disputes that there is a reasonable expectation of success in combining the references. The device isolation film of *Hemmenway* is formed by a LOCOS method, which covers the active region including the source/drain regions 42

and 43 and is used as a gate oxide film. The LOCOS layer 25 is the first structure to be formed on the substrate and requires an additional etching step to expose the source/drain regions in order to form a silicide layer, which prevents the formation of a silicide layer on the source/drain regions. Although *Wu* discloses a silicide layer on the source/drain regions and the top surface of the gate electrode, one of ordinary skill in the art would not expect that combining *Hemmenway* with *Wu* would produce the claimed combination. In fact, one of ordinary skill would realize that the combination of *Wu* with *Hemmenway* is not possible.

Rejection over *Youn* in view of *Wu*

Youn discloses a method for forming a field effect transistor. The method includes disposing silicide layer 28a on the sidewall of source/drain regions 27a and 27b, and the top surface of gate electrode 24. (*Youn*, col. 3, ll. 49–52; Figures 3B, 4D, and 5D.)

Youn's silicide layer on the sidewall of the source/drain regions and the top surface of the gate electrode and a *Wu's* first silicide layer on a source drain region, in turn, on SOI structure (as discussed above), however, are different from, "a first silicide layer disposed at an *interface of the impurity junction region and the device isolation film*," as recited in claim 1 (emphasis added), which further recites, "a device isolation film disposed in the second silicon layer, wherein the device isolation film defines an active region of the SOI wafer." Consequently, combination *Youn* with *Wu* fails to teach or suggest at least, "a first silicide layer disposed at an interface of the impurity junction region and the device isolation film," as recited in claim 1.

Applicant also disputes that there is a reasonable expectation of success in combining the references. In *Youn*, the source/drain regions 27a and 27b protrude above the device isolation film 22; thus it is not possible to modify *Youn*, whether or not in combination with *Wu*, to include "a first silicide layer disposed at an interface of the impurity junction region and the device isolation film." Therefore, one of ordinary skill in the art would not expect that combining *Youn* with *Wu* would result in the claimed combination.

Because the combinations of *Hemmenway* with *Wu* and *Youn* with *Wu* both fail to teach or suggest each claim element, including at least "a first silicide layer disposed at an *interface of the impurity junction region and the device isolation film*," and there is no reasonable expectation of successfully combining the references to achieve the claimed combination, Applicant submits claim 1 is allowable over these references. Applicant submits that claim 2 is likewise allowable at least because of its dependence from allowable claim 1. Applicant therefore requests the withdrawal of the rejection of these claims and their timely allowance.

Applicant also notes that although the Examiner referred to U.S. Patent 4,839,309 ("*Easter*"), the Examiner did not apply that reference or set forth any of the three elements necessary for a rejecting any claim in view of that reference.

In view of the foregoing, Applicant respectfully requests reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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